REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

A minor formal change is made to the specification.

Minor formal changes are also made to the claims.

Claims 1-20 are present in this application. Claims 1, 7-11, 12, 13, and 18-20 are rejected under 35 U.S.C. §102(b) over U.S. 4,145,739 (Dunning et al.) and claims 3-6, 14-16 are rejected under 35 U.S.C. §103(a) over Dunning et al. in view of U.S. 5,822,779 (Intrater et al. ).

The present invention is directed to a processor having a processor core, an extension unit and a direct memory access controller connected to both the processor core and the extension unit. In other words, these elements are found in a single processor. In one example of the present invention, the processor is integrated on a semiconductor chip, that is, the processor core, extension unit and direct memory access controller are all integrated on one semiconductor chip.

Turning to the prior art rejections, the Office Action rejects claim 1 over Dunning et al. However, Dunning et al. is directed to a processor system having a plurality of processors. There is no disclosure or suggestion of a processor having a processor core, extension unit and direct memory access controller. The "extension unit" identified in the Office Action as the work station unit 10, is separate from the master 16 (see Fig. 1). Clearly, Dunning does not anticipate claim 1 and the rejection based thereon must be withdrawn.

Claim 12 recites the processor core, extension unit and direct memory access controller are all integrated on one semiconductor chip. This clearly not the case with Dunning et al. where the "extension unit" is identified as the work station unit 10, separate from the master 16. Moreover, there is no disclosure of a processor integrated on a semiconductor chip. Dunning et al., directed to a processor system having a plurality of

processors, clearly does not disclose a processor having the elements recited in claim 12 integrated on one semiconductor chip. The rejection of claim 12 also must be withdrawn since Dunning et al. does not disclose the elements of claim 12.

Claims 3-6 and 14-16 were rejected over Dunning et al. in view of Intrater et al. As discussed above, there is no suggestion in Dunning et al. of the processor of claims 1 or 12. Intrater et al. is relied upon for a system including a decode and control circuit for resetting a CPU core. The system is asserted to have the ability to "set and reset the CPU core" which could be achieved by "reconfiguring the control parameters of Intrater (e.g. the clock reset) into Dunning so that the specific clock disabling signal of Intrater could be recognized by Dunning." However, there is no such description of such a system in Intrater et al., in particular even in the portion referred to by the Examiner (column 5, lines 25-40). Moreover, the operation of resetting a CPU is different from the operation of halting a clock signal for the processor core. The purpose of resetting a CPU is not the same as the purpose of halting a clock signal for the processor core.

Even combining Intrater et al. with Dunning et al. would not cure the deficiencies of Dunning et al. Further, Intrater et al. also does not suggest the systems of claims 3-6 and 14-16. The rejection of claims 3-6 and 14-16 over Dunning et al. and Intrater et al. must also be withdrawn.

It is respectfully submitted that the present application is in condition for allowance, and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Carl E. Schlier
Registration No. 34,426

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)